Amendments to the Claims

1. (cancelled)

2. (currently amended) A method of adapting synchronous time division multiplexed (TDM) traffic at an interface between a synchronous network in which the traffic is transported in frames and an asynchronous network in which ~~the~~ adapted traffic is transported in cells, the method comprising generating pointers identifying phase of the TDM traffic, mapping said synchronous frames into primary multiplexed groups, mapping each said primary multiplexed group into traffic cells in a respective asynchronous virtual circuit, and wherein said pointers are mapped into one or more separate asynchronous cells for transport ahead of said traffic cells.

3. (original) A method as claimed in claim 2, wherein said primary multiplexed groups are multiplexed by byte interleaving into a secondary multiplexed signal.

4. (previously presented) A method as claimed in claim 3, wherein said asynchronous network is an ATM network carrying ATM cells and said adaptation is performed using ATM adaptation layer zero (AAL0).

5. (currently amended) A method as claimed in claim 4, wherein a time slot group frame boundary coincides with ~~the~~ a start of an ATM cell.

6. (previously presented) A method as claimed in claim 2, wherein each cell containing time slots from a synchronous frame is given its own virtual channel indicator, and wherein cells relating to that frame are allocated a common virtual path indicator so that said cells can be transmitted and switched together.

7. (cancelled)

8. (cancelled)

9. (currently amended) An arrangement for adapting synchronous time division multiplexed (TDM) traffic at an interface between a synchronous network in which ~~the~~ traffic is transported in synchronous frames and an asynchronous network in which ~~the~~ adapted traffic is transported in cells, the arrangement comprising means for generating pointers identifying phase of the TDM traffic, mapping means for mapping said synchronous frames into primary multiplexed groups and for mapping each said primary multiplexed group into traffic cells in a respective asynchronous virtual circuit, and wherein said pointers are mapped into one or more separate asynchronous cells for transport ahead of said traffic cells.

10. (previously presented) An arrangement as claimed in claim 9, and including means for multiplexing said primary multiplexed groups by byte interleaving into a secondary multiplexed signal.

11. (previously presented) An arrangement as claimed in claim 9, wherein each cell containing time slots from a synchronous frame is given its own virtual channel indicator, and wherein cells relating to that frame are allocated a common virtual path indicator so that said cells can be transmitted and switched together.

12. (previously presented) An arrangement as claimed in claim 9, and provided in the form of an integrated circuit.

13. (previously presented) An arrangement as claimed in claim 9, wherein said asynchronous network is an ATM network carrying ATM cells.

14. (currently amended) A method as claimed in claim 2, wherein each of the frames ~~each~~ comprises a plurality of time slots, the interface comprises a timing

reference and wherein the pointers identify ~~the number of~~ ~~the~~ first time slots in the frames relative to the timing reference.

15. (currently amended) An arrangement as claimed in claim 9, wherein each of the frames ~~each~~ comprises a plurality of time slots, the arrangement comprises a timing reference and the means for generating pointers is arranged to generate pointers identifying ~~the~~ first time slots in the frames, relative to the timing reference.